Notice of Allowability	Application No.	Applicant(s)	
	10/673,966	HENNINGER ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the 01-06-2005 interview*.

2. ☒ The allowed claim(s) is/are *1-11*.

3. ☒ The drawings filed on *29 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/27/04 & 9/29/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20050106* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SHOUXIANG HU
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Laurence A. Greenberg (RN: 29,308) and Gregory Mayback (RN: 40,719) on January 6, 2005.

The application has been amended as follows:

IN THE CLAIMS

1. (Currently Amended) A trench transistor, comprising:

a semiconductor body of a first conduction type having a surface region;

a semiconductor region of a second conduction type ~~opposing~~ opposite to said first conduction type provided in said surface region of said semiconductor body and having ~~an uncovered~~ a top surface ~~defining a top~~;

a trench formed in said semiconductor body and said semiconductor region ~~having a trench formed therein~~ and extending from said top ~~downward from said uncovered~~ surface of said semiconductor region ~~through~~ to a level below said semiconductor region ~~as far as said semiconductor body~~, said trench having a wall, a lower region, and an upper region;

an insulation layer at least partially lining said wall of said trench and having an upper end;

a conductive trench filling disposed in said lower region of said trench and having a top side;

an insulating trench filling disposed in said upper region of said trench, having a top surface, and adjoining said top side of said conductive trench filling; and

a semiconductor zone of said first conduction type provided along said insulation layer in said semiconductor region and having a lower edge;

said upper end of said insulation layer and said top surface of said insulating trench filling at least partially ~~projecting~~ disposed above said surface of said semiconductor region;

said lower edge of said semiconductor zone being curved and lying lower than said top side of said conductive trench filling;

a spacer provided along said insulation layer and ~~projecting~~ disposed above said top surface of said semiconductor region and serving as a dopant source for said semiconductor zone; and

a channel zone running along said insulation layer in said semiconductor region.

2. (Currently Amended) The trench transistor according to claim 1, wherein said top surface of said semiconductor region has ~~a~~ an additional trench formed between two cells.

3. (Currently Amended) The trench transistor according to claim 1, further comprising a silicide layer ~~making~~ in contact ~~between~~ with said semiconductor region and said semiconductor zone.

4. (Original) The trench transistor according to claim 1, wherein said semiconductor region has a contact zone.

5. (Original) The trench transistor according to claim 4, wherein said contact zone is implanted.

6. (Original) The trench transistor according to claim 1, further comprising an insulating spacer layer underlying said spacer.

7. (Original) The trench transistor according to claim 1, wherein said spacer is made of a material selected from the group consisting of polycrystalline silicon, a metal provided with dopant, borophosphosilicate glass, phosphosilicate glass, and borosilicate glass.

8. (Original) The trench transistor according to claim 6, wherein said insulating spacer layer is made of a material selected from the group consisting of silicon nitride and silicon oxide.

9. (Original) The trench transistor according to claim 1, wherein said semiconductor body is made from a material selected

from the group consisting of silicon, silicon carbide, and a compound semiconductor.

10. (Currently Amended) The trench transistor according to claim 1, further comprising ~~further~~ additional electrodes disposed in said trench.

11. (Original) The trench transistor according to claim 1, further comprising a field plate disposed in said trench.

12-23. (Cancelled)

Allowable Subject Matter

Claims 1-11 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: Prior art does not teach or render obvious a trench transistor as defined in the above allowed claims, comprising particularly: a trench formed in a semiconductor body of a first conductivity type and extending from a top surface of a semiconductor region of a second

conductivity type in the surface region of the semiconductor body to a level below the semiconductor region; an insulation layer lining at least part of the wall of the trench and extending to above the top surface of the semiconductor region; a conductive trench filling disposed in the lower portion of the trench; an insulating trench filling disposed in the upper region of the trench; a semiconductor zone of the first conduction type provided in the semiconductor region along the insulation layer; a spacer provided along the insulation layer above the top surface of the semiconductor region and serving as a dopant source for the semiconductor zone; and a channel zone running along the insulation layer in the semiconductor region, wherein the lower edge of the semiconductor zone is curved and lies lower than a top side of the conductive trench filling.

In Murakami (US 5,177,572) provided in the 09-27-04 IDS, as an example from the relevant prior art references, the trench transistor shown in Fig. 7 has a semiconductor zone (3) having a flat lower edge, and lacks an equivalent semiconductor region with a conductivity type opposite to that of the semiconductor zone. And, references A-D cited in this Office action each lack a spacer that serves as a dopant source for an equivalent surface semiconductor zone.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A-D are cited as being related to a trench transistor structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
January 6, 2005

SHOUXIANG HU
PRIMARY EXAMINER